Transistor Sizing for High Performance and Low Power

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Abstract

Tuning a circuit by adjusting individual transistor sizes offers higher performance and lower power, for circuits with up to hundreds of thousands of transistors, than the best that can be achieved with standard cells: Typically, at the same clock rate, power can be cut in half. At the same power, clock rate can be increased 25%.

1 Introduction

In recent years, the joint optimization of performance and power consumption in VLSI circuits has taken on increased importance, fueled by two market trends. First is the great expansion in portable products that must rely on battery power. Second is the large increase in power consumption of high-end microprocessors, due to increasing clock rates and scale of integration. The product that exemplifies both these trends is the laptop PC, which with current technology suffers from a combination of poor performance, heavy batteries, and limited charge lifetime. An improved delay-vs.-power tradeoff curve is an important asset in today's VLSI markets, and will increase in importance as line widths continue to decrease.

Both the power and maximum clock rate of a sequential circuit can be controlled by varying the sizes (channel widths) of the transistors. The sum of transistor sizes gives a rough estimate of power consumption, but delay depends nonlinearly on transistor sizes: Doubling a transistor's size halves the time for it to drive a load, but slows down its input. The problem can be formalized fairly simply: Given a synchronous circuit with N transistors of sizes $x_1, x_2, \ldots, x_N$, find values for the x_i that jointly minimize the power consumption and the smallest clock period at which the circuit will operate correctly.

TILOS (TImed LOgic Synthesizer, pronounced *tee-los*) [4] [6], is a program that accepts a transistor-level connectivity file and a performance-specification file, and adjusts transistor sizes and permutes series-connected networks within complex logic gates to meet the user's performance specification while simultaneously minimizing power consumption. This paper relates experiences applying TILOS to various commercial circuits, and the enhancements necessary to accommodate these circuits.

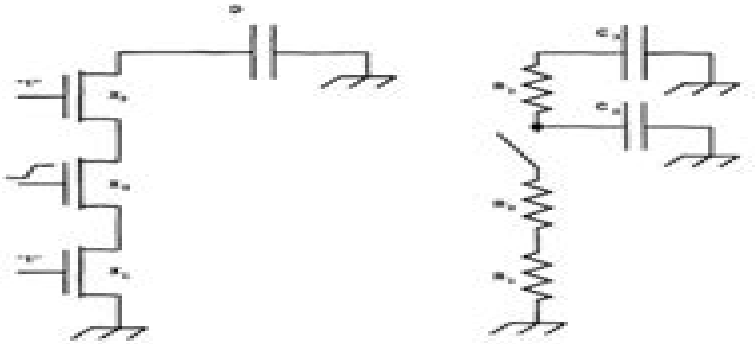

Figure 1: A pulldown network is modeled by an equivalent RC network.

2 Timing Model

TILOS models a transistor as a perfect switch in series with a linear resistor. The gate, source, and drain capacitances are proportional to transistor size X_i, and the transistor resistance is inversely proportional to X_i.

Figure 1 illustrates the modeling of a pulldown network by an equivalent RC network. The delay is modeled by Elmore delay [9], which in this case is

$$(R_1 + R_2)C_2 + (R_1 + R_2 + R3)C_3. \qquad (1)$$

Given that each terminal capacitance is proportional to transistor size, and resistance is inversely proportional to transistor size, (1) can be rewritten in terms of the transistor sizes X_1, X_2, and X_3. Each R_i is proportional to $1/X_i$, and each C_i is some constant (for wire capacitance) plus one term for each transistor terminal incident on the node. Each of these terms is proportional to transistor size. (1) can then be rewritten as

$$(A/X_1 + A/X_2) * (B * X_2 + B * X_3 + C) + (A/X_1 + A/X_2 + A/X_3) * (B * X_3 + D) \qquad (2)$$

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