

Functional Verification Methodology for the PowerPC 604™ Microprocessor

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Abstract

Functional (i.e., logic) verification of the current generation of complex, super-scalar microprocessors such as the PowerPC 604™ microprocessor presents significant challenges to a project's verification participants. Simple architectural level tests are insufficient to gain confidence in the quality of the design. Detailed planning must be combined with a broad collection of methods and tools to ensure that design defects are detected as early as possible in a project's life-cycle.

This paper discusses the methodology applied to the functional verification of the PowerPC 604 microprocessor.

1. Introduction

Only in recent years have industry practitioners begun publishing information detailing functional verification practices and procedures [1, 2, & 3]. Building on work previously published describing the PowerPC 604 microprocessor project [4 & 5], this paper describes the functional verification methodology employed. The design methodology and specification approach are briefly discussed. Practices covering project and verification planning, testcase generation, simulation, coverage assessment, and design quality confidence are included. Finally, possibilities for future improvements to these functional verification practices are examined.

The term "verification methodology" used in this paper should be interpreted to mean "an integrated set of techniques and methods applied to produce a defect-free microprocessor design".

2. Design Methodology and Specification Approach

At the Somerset Design Center, methods and tools used in the microprocessor verification effort are significantly influenced by the tools used to develop the design model.

2.1 Development and Design Modeling

The selected hardware design modeling language (HDL) now entrenched in the design process is a proprietary superset of the Verilog language. Depending upon how a design is partitioned, portions of the logic and physical design may be synthesized while other portions may be constructed as custom logic and layout in a traditional manner. The logical and physical design characteristics can then be analyzed in parallel.

The design's logic characteristics are examined from the perspective of functional logic -- "Does the design correctly execute according to the architectural and implementation-dependent design specifications?". For the PowerPC 604 microprocessor project, design description was captured at the gate and logic device levels. Using a variety of tools for compilation and translation, models were produced in forms usable by multiple simulation systems including a Verilog event-driven simulator and proprietary cycle based simulators. Simulation was performed to verify the correctness of the simulation model.

The design's physical characteristics were examined from the perspective of physical circuit design -- "Does the design correctly meet desired timing and electronic specifications (i.e., set-up and hold constraints, switching speeds, power consumption, etc.).

An equivalency check, shown in Figure 1, was performed periodically to ensure that the hardware technology description of the design was synchronized with the high-level logical description.

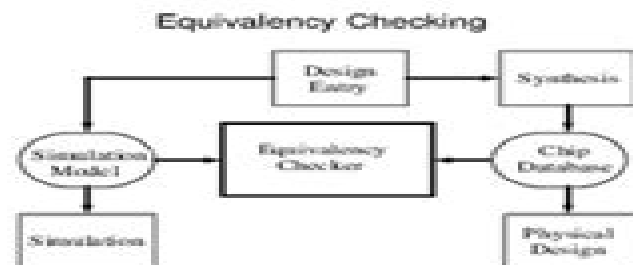


Figure 1: Equivalency Check and Logical/Physical Views

Figure 2 illustrates the design process used by the PowerPC 604 microprocessor project. It resembled a spiral-type software development approach. Most project effort involved two (iterative) steps:

- improve design, and
- evaluate improvements;

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Mielenz, 2009-01-27 Die vorliegende Arbeit untersucht die Eignung datenbasierter Modellierungsmethoden in Anwendung auf die Verhaltensmodellierung in der Automobilelektronik. Für die Untersuchung werden zwei Anwendungsgebiete vorgestellt. Einerseits wird die automatisierte Generierung funktionaler Verhaltensmodelle für Mixed Signal Systeme analysiert, andererseits die Anwendung datenbasierter Modelle für die Signalanalytik integrierter Sensorsysteme evaluiert. Die Untersuchungen zur automatisierten Erstellung von funktionalen Verhaltensmodellen basieren auf einer Nutzwertanalyse, die gängige Verfahren der Verhaltensmodellierung vorstellt und qualitativ diskutiert. In diesem Zusammenhang werden Bewertungskriterien abgeleitet, die im Verlauf der Arbeit zur Beurteilung der entwickelten Methodik eingesetzt werden. Das entwickelte Verfahren ermöglicht eine automatische Erstellung von funktionalen Verhaltensmodellen für Systeme, die in einer simulierbaren Implementierung vorliegen. Durch eine systemtheoretische Betrachtung der Signalverläufe können Komponenten aus unterschiedlichen physikalischen Domänen berücksichtigt werden. Zur Abbildung nichtlinearer Zusammenhänge wird auf Support Vektor Maschinen zurückgegriffen, die für die Repräsentation dynamischer Informationen um eine Funktionsbibliothek erweitert werden. Grundsätzlich für die erfolgreiche Umsetzung des gesamten Prozesses ist das Vorhandensein einer transienten Datenbasis, die aus Simulationen der Originalsysteme gewonnen werden. Für die Erstellung dieser Daten wird ein Konzept vorgeschlagen, das Methoden des experimentellen Designs und des aktiven Lernens vereint. Um eine breite Anwendung der generierten Modelle in diversen Simulatoren zu ermöglichen, wird ein C-basiertes Schnittstellenkonzept vorgestellt, das die Einbindung eines generierten Modells in die Simulatoren AdvanceMS, Saber und Simulink automatisiert. Als Evaluationsbeispiele dienen eine Ladungspumpe, eine Einspritzdose und ein Drucksensormodell. Das zweite Anwendungsfeld thematisiert die Realisierung einer softwarebasierten Signalanalytik für einen integrierten Gassensor. Mittels experimenteller Daten werden für die Signalanalytik automatisiert datenbasierte Modelle erstellt, womit der Aufwand einer traditionellen Software-Implementierung reduziert werden kann. Damit sich die untersuchte Methodik für die Verwendung in kostengünstigen Produkten qualifiziert, müssen die Speicheranforderungen des datenbasierten Modells an die Randbedingungen eines Mikrocontrollers angepasst werden. Für diese Anforderungen wird ein neues Lernverfahren für diskretisierte Support Vektor Maschinen vorgestellt, das ohne merkliche Einbußen in der Genauigkeit eine Reduktion des Speicherbedarfs ermöglicht.

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