

TEST CIRCUIT STRUCTURES FOR CHARACTERIZING THE EFFECTS OF LOCALIZED HOT-CARRIER-INDUCED CHARGE IN VLSI SWITCHING CIRCUITS*

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Abstract

Data are presented that were collected from test circuit structures that were hot-carrier-stressed under conditions existing in actual VLSI switching circuits. It is shown that the localized nature of hot-carrier-induced damage to n-channel MOSFETs must be considered to accurately model these data by computer circuit simulations.

1. Introduction

Hot-carrier-induced degradation is a long-term reliability issue in scaling n-channel MOS devices. Many studies have provided data on the degradation of discrete device parameters; however, the relationship between the degradation of these parameters and circuit performance has not been shown. A further complication of this relationship is that the charge induced in the device by hot-carrier injection is localized in one region of the channel [1,2]. Consequently, the device no longer exhibits symmetric dc characteristics [3,4]. The effect of this asymmetry on switching performance in VLSI circuits has received little attention [5,6]. The method of assessing circuit performance degradation has been limited to simulating circuits with worst-case arbitrarily selected shifts in the n-channel device's threshold voltage and transconductance. This method of modeling does not account for the spatial distribution of hot-carrier-induced damage.

This paper presents results obtained from a CMOS test chip that was used to study the hot-carrier effects on digital switching time of inverters and transmission gates. The test chip contains test circuits configured as CMOS inverters, transmission gates, and other dynamic circuit structures. The MOSFETs within the circuits could be probed so the degradation of their dc characteristics could be directly measured. These circuit structures were hot-carrier-stressed under pulsed switching conditions similar to their operation in VLSI circuits.

Section II describes the test circuit structures included on the test chip. The experimental procedures and test conditions used to stress and collect data are shown. Section III presents experimental results showing the effect of the stress on the dc characteristics of the MOSFETs in the test circuits. The effect of the localized nature of the hot-carrier-induced charge on digital switching time is shown to have a strong dependence on the circuit configuration. Section IV describes a simple model that was used in computer circuit simulations to model the localized effect of the charge on digital switching performance.

II. Experimental Details

A CMOS test chip containing test circuits configured as CMOS inverters, transmission gates, and dynamic shift registers was fabricated by the MOSIS foundry system [7]. The MOSFETs comprising the transmission gate circuits had effective channel lengths of 1.8 μm and widths of 20 μm . The p-channel MOSFET in the inverters had a width of 40 μm .

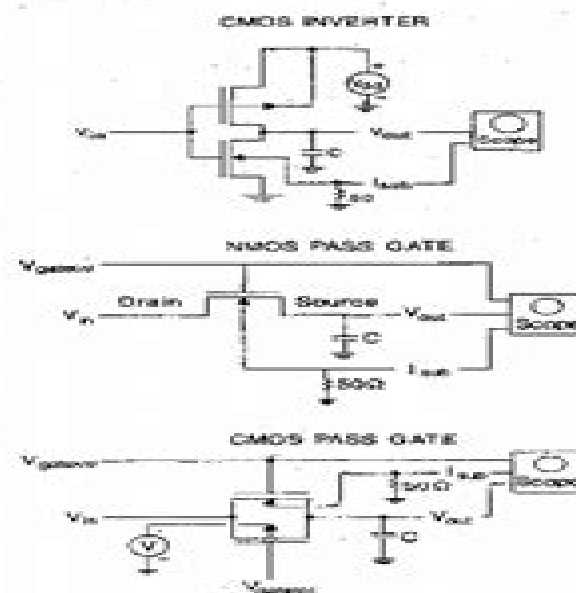


Figure 1. Measurement setup for transient substrate current generated by CMOS inverter (top), NMOS transmission gate (center), and by CMOS transmission gate (bottom).

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