

A photograph of a large conference hall during the International Test Conference 2023. A speaker in a blue shirt stands at a podium on the right, addressing the audience. The audience is seated at long tables covered with blue cloths, arranged in rows. The hall is filled with people, and the atmosphere appears professional and engaged.

# INTERNATIONAL TEST CONFERENCE 2023

October 8-13, 2023

# Proceedings International Test Conference 1999

**IEEE, IEEE Laser and Electro-Optics  
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## **Proceedings International Test Conference 1999:**

*Untersuchungen der Kontakteigenschaft beim Testen von integrierten Schaltungen* Markus Reinl, 2009-01-27 Diese Arbeit beschäftigt sich mit den Kontakteigenschaften beim Testen von integrierten Schaltungen. Der Schwerpunkt liegt darauf ein besseres Verständnis für die Mechanismen und physikalischen Eigenschaften des elektrischen und mechanischen Kontaktes zwischen den Probing Nadeln und den Pads zu erhalten. Entscheidend dabei ist der Zusammenhang zwischen elektrischem Kontaktwiderstand und den auftretenden mechanischen Kräften. Um die einwirkenden Kräfte in normaler und lateraler Richtung und den elektrischen Widerstand in situ und unter Echtzeitbedingungen zu messen, ist ein spezieller Messplatz entwickelt und aufgebaut worden. Durch die stetige Erhöhung der Integrationsdichte werden bei aktuellen Produkttechnologien die Probing Pads über aktives Schaltungsgebiet gelegt, um weitere Chipfläche einzusparen. Dadurch kommt es vermehrt zu Ausfällen der getesteten Schaltungen, da die Isolationsschichten zwischen den Metallisierungsebenen aufgrund des Kräfteintrages durch die Probing Nadeln mechanisch zerstört werden. Eine Reduzierung der einwirkenden Kräfte bedingt in der Regel eine Verschlechterung des elektrischen Kontaktwiderstandes. Mit dem in dieser Arbeit entwickelten Messplatz wird der Zusammenhang zwischen mechanischen und elektrischen Kontakteigenschaften untersucht. Dabei hat sich herausgestellt, dass das natürliche Aluminiumoxid auf den Probing Pads nicht den alleinigen Grund für eine Verschlechterung des Kontaktwiderstandes darstellt, wie häufig in Veröffentlichungen nachzulesen. Die Messungen haben gezeigt, dass auf Aluminium ein vergleichbarer elektrischer Kontaktwiderstand wie auf Gold erreicht werden kann. Jedoch sind die auftretenden Kräfte bei gleichen Bedingungen auf Aluminium höher. Mit dem Ziel, den Kräfteintrag bei gleich bleibendem Widerstand zu reduzieren, sind verschiedene Reinigungsverfahren zur Entfernung der Aluminiumoxidschicht evaluiert worden. Dabei zeigte sich, dass eine Entfernung des Oxides mit den untersuchten Verfahren nur schwer möglich ist. Ferner haben Messungen gezeigt, dass durch eine Entfernung des Oxides und anschließende saubere Oxidation keine Verbesserung der Kontakteigenschaften erzielt werden kann. Untersuchungen von Wafern aus der industriellen IC Produktion haben verdeutlicht, dass aufgrund des Herstellungsprozesses mit zusätzlichen Kontaminationen auf der Padoberfläche zu rechnen ist. Entsprechende XPS Analysen veranschaulichen, dass ein erheblicher Anteil an Fluorkontaminationen auf der Oberfläche zu finden ist. In Verbindung mit den durchgeführten Probing Versuchen zur Bestimmung der Parameter Kontaktwiderstand und Kraft, kann ein direkter Zusammenhang zwischen Fluorkontaminationen und elektrischem Kontaktwiderstand hergestellt werden. Durch die Kontaminationen bildet sich eine isolierende Schicht zwischen Probing Nadel und Padoberfläche, was zu einem gravierenden Anstieg des Widerstandes führt. Die Betrachtung der theoretischen Beschreibung des elektrischen Kontaktwiderstandes bestätigt die experimentell erzielten Ergebnisse. Der Widerstandswert wird hauptsächlich durch das Vorhandensein von Verunreinigungen auf der Oberfläche beeinflusst. Aus diesem Grund beschäftigt sich die Arbeit im Weiteren mit möglichen Verfahren zur Entfernung der Kontaminationen. Ausgehend von den durchgeführten

hrten Untersuchungen werden sowohl trockenchemische Plasmaprozesse wie auch nasschemische Prozesse n her betrachtet Eine M glichkeit stellt die Zugabe von Wasserstoff direkt zu dem Fluorplasma dar durch das die Verunreinigungen verursacht werden Die Wafer werden praktisch w hrend der Prozessierung einem in situ HF Dip unterzogen wodurch die Kontaminationen verringert werden und somit eine Verbesserung des Kontaktwiderstandes erzielt wird Die nachtr gliche Behandlung von verunreinigten Proben durch ein Sauerstoffplasma f hrt zu einer Verbesserung der Kontakteigenschaften da die Fluorkontaminationen reduziert werden Zus tzliche Experimente mit einem reinen Wasserstoffplasma zeigen ebenfalls gute Ergebnisse hinsichtlich einer Verbesserung der Probing Eigenschaften Durch die nasschemische Reinigung mit Tetrachlorethylen kann ebenfalls eine Verbesserung des Kontaktwiderstandes realisiert werden jedoch bei ansteigenden Kr ften Die in dieser Arbeit zusammengefassten Ergebnisse zeigen deutlich dass ein direkter Zusammenhang zwischen Verschlechterung der Kontakteigenschaften und Fluorkontaminationen besteht Mit den untersuchten Reinigungsverfahren k nnen diese entfernt und eine Verbesserung der Performance beim Probing erzielt werden

*SOC (System-on-a-Chip) Testing for Plug and Play Test Automation* Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing

*Power-Aware Testing and Test Strategies for Low Power Devices* Patrick Girard, Nicola Nicolici, Xiaoqing Wen, 2010-03-11 Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry Elaborate power management strategies such as dynamic voltage scaling clock gating or power gating techniques are used today to control the power dissipation during functional operation The usage of these strategies has various implications on manufacturing test and power aware test is therefore increasingly becoming a major consideration during design for test and test preparation for low power devices This book explores existing solutions for power aware test and design for test of conventional circuits and systems and surveys test strategies and EDA solutions for testing low power devices

**Proceedings, International Test Conference 1996**, 1996 ITC is the World s largest premier technical conference on the testing and total quality of integrated electronics and the assenblies and systems that are based on them Proceedings, 2003 Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the

complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions

**Advances in Electronic Testing** Dimitris Gizopoulos, 2006-01-22 Advances in Electronic Testing Challenges and Methodologies is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing The book is a comprehensive elaboration on important topics which capture major research and development efforts today The motivation and inspiration behind this book is to deliver a thorough text that focuses on the evolution of test technology provides insight about the abiding importance of discussed topics records today s state of the art and industrial practices and trends reveals the challenges for emerging testing methodologies and envisages the future of this journey The book consists of eleven edited chapters written by experts in Defect Oriented Testing Nanometer Technologies Failures and Testing Silicon Debug Delay Testing High Speed Test Interfaces DFT Oriented Low Cost Testers Embedded Cores and System on Chip Testing Memory Testing Mixed Signal Testing RF Testing and Loaded Board Testing Contributing authors are affiliated with in alphabetical order Agilent ARM Balearic Islands Univ IBM Inovys Intel LogicVision Magma Mentor Graphics New Mexico Univ Sandia National Labs Synopsys Teradyne and Texas Instruments Advances in Electronic Testing Challenges and Methodologies is an advanced textbook and reference point for senior undergraduate and graduate students in MSc or PhD tracks professors and research leaders in the electronic testing domain It is also for industry design and test engineers and managers seeking a global view and understanding of test technology practices and methodologies and a dense elaboration on test related issues they face in their development projects There is a definite need for documenting the advances in testing I find the work of this edited volume by Dimitris Gizopoulos and his team of authors to be significant and timely the book provides besides novel test methodologies a collective insight into the emerging aspects of testing This I think is beneficial to practicing engineers and researchers both of whom must stay at the forefront of

technology This latest addition to the Frontiers Series is destined to serve an important role From the Foreword by Vishwani D Agrawal Consulting Editor Frontiers in Electronic Testing Book Series Proceedings, International Test Conference 1997 ,1997 IEEE VLSI Test Symposium ,2005 **Proceedings of the ... International Symposium on the Physical & Failure Analysis of Integrated Circuits** ,2005 **Proceedings of the IEEE 1999 Custom Integrated Circuits Conference** ,1999 18th IEEE VLSI Test Symposium ,2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test compaction and design validation analog BIST and functional test and verification issues Also covered are STIL extension IDDQ test and on line testing and fault tolerance Lacks a subject index Annotation copyrighted by Book News Inc Portland OR **Proceedings** VHDL International. Users Forum,2000 **Fault Modeling and On-line Testing for Deep-submicron Noise Interference in System-on-chips** Yi Zhao,2004 **Proceedings** ,1999 19th IEEE VLSI Test Symposium ,2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc IC Test Using the Energy Consumption Ratio Wanli Jiang,2000 **2002 IEEE 16th Annual Meeting Lasers and Electro-Optics Society** IEEE,IEEE Laser and Electro-Optics Society Staff,2003-12 Digest of Technical Papers ,2001 **Asian Test Symposium** ,2005

## Whispering the Secrets of Language: An Emotional Quest through **Proceedings International Test Conference 1999**

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