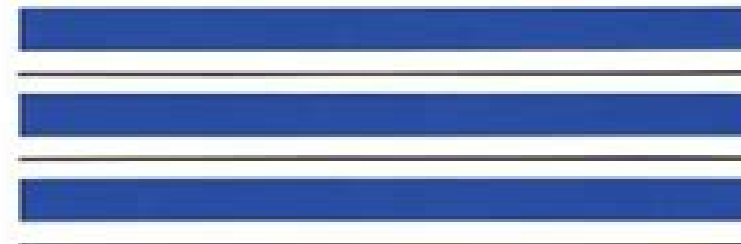

SIMULATION TECHNIQUES AND SOLUTIONS FOR MIXED-SIGNAL COUPLING IN INTEGRATED CIRCUITS

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Simulation Techniques And Solutions For Mixed Signal Coupling In Integrated Circuits

VM Jensen



Simulation Techniques And Solutions For Mixed Signal Coupling In Integrated Circuits:

Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits Nishath K. Verghese, Timothy J. Schmerbeck, David J. Allstot, 2012-12-06 The goal of putting systems on a chip has been a difficult challenge that is only recently being met Since the world is analog putting systems on a chip requires putting analog interfaces on the same chip as digital processing functions Since some processing functions are accomplished more efficiently in analog circuitry chips with a large amount of analog and digital circuitry are being designed Whether a small amount of analog circuitry is combined with varying amounts of digital circuitry or the other way around the problem encountered in marrying analog and digital circuitry are the same but with different scope Some of the most prevalent problems are chip package capacitive and inductive coupling ringing on the RLC tuned circuits that form the chip package power supply rails and off chip drivers and receivers coupling between circuits through the chip substrate bulk and radiated emissions from the chip package interconnects To aggravate the problems of designers who have to deal with the complexity of mixed signal coupling there is a lack of verification techniques to simulate the problem In addition to considering RLC models for the various chip package board level parasitics mixed signal circuit designers must also model coupling through the common substrate when simulating ICs to obtain an accurate estimate of coupled noise in their designs Unfortunately accurate simulation of substrate coupling has only recently begun to receive attention and techniques for the same are not widely known Simulation Techniques and Solutions for Mixed Signal Coupling in Integrated Circuits addresses two major issues of the mixed signal coupling problem how to simulate it and how to overcome it It identifies some of the problems that will be encountered gives examples of actual hardware experiences offers simulation techniques and suggests possible solutions Readers of this book should come away with a clear directive to simulate their design for interactions prior to building the design versus a build it and see mentality EDA for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno, Louis Scheffer, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The second volume EDA for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic to GDSII a file format used to transfer data of semiconductor physical layout analog mixed signal design physical verification and technology CAD TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale power supply network design and analysis design modeling and much more Save on the complete set Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data

of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **Proceedings of the IEEE**

1999 Custom Integrated Circuits Conference, 1999 System Level Mixed Signal Design with Analog Platforms Fernando De Bernardinis, 2005 *IEEE Circuits & Devices*, 2006 1996 IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design Franco Maloberti, Andrea Baschirotto, Valentino Liberali, 1996 **Synthesis of Power Distribution to Manage Signal Integrity in Mixed-Signal ICs** Balsha R. Stanisic, Rob A. Rutenbar, L. Richard Carley, 1996-05-31 The move to higher levels of integration has increased the fraction of application specific integrated circuit ASIC designs containing both analog and digital circuits While the die area for the analog portion of these chips is modest the design time is often significant This has motivated the development of automated analog physical design tools for cell level place and route and system level signal integrity routing To date there is no tool that has specifically addressed the critical design task of synthesizing the power distribution for the analog portion of an analog or mixed signal ASIC Synthesis of Power Distribution to Manage Signal Integrity in Mixed Signal ICs describes algorithms for analog power distribution synthesis and demonstrates their effectiveness Existing digital power bus synthesis algorithms have failed to address critical concerns for analog circuitry thus yielding unacceptable results These tools synthesize only the bus component of power distribution networks and only consider simplified DC aspects of macros and busses Readers of the companion book in this series Simulation Techniques and Solutions for Mixed Signal Coupling in Integrated Circuits Kluwer Academic Publishers already recognize the inadequacy of this simplified view of the noise and power distribution problem in mixed signal integrated circuits Synthesis of Power Distribution to Manage Signal Integrity in Mixed Signal ICs addresses power distribution synthesis for mixed signal integrated circuits Several key challenges in power distribution design are identified and automated methods to overcome them are described This book presents a new formulation for the analog power distribution synthesis problem which synthesizes both the power busses power I O cell assignment by evaluating DC AC and transient interaction between the macros busses chip substrate and package Furthermore algorithms are introduced which

simultaneously optimize power I O cell assignment macro cell substrate coupling power bus topology selection and power bus sizing Synthesis of Power Distribution to Manage Signal Integrity in Mixed Signal ICs will be of interest to CAD designers and researchers specializing in physical design modelling and circuit synthesis **IEICE Transactions on Electronics** ,2005 **BMAS ...** ,2003 **Proceedings** ,2004 **IEEE Transactions on Circuits and Systems** ,2006 **Digest of Technical Papers** ,2001 **VLSI: Systems on a Chip** Luis Miguel Silveira,Srinivas Devadas,Ricardo A. Reis,1999-12-31 The current trend towards the realization of complex and versatile Systems on a Chip requires the combined efforts and attention of experts in a wide range of areas including microsystems embedded hardware software systems dedicated ASIC and programmable logic hardware reconfigurable computing wireless communications and RF issues video and image processing memory systems low power design techniques design test and verification algorithms modeling and simulation logic synthesis and interconnect analysis Thus the contributions presented herein address a wide range of Systems on a Chip problems VLSI Systems on a Chip comprises the selected proceedings of the Tenth International Conference on Very Large Scale Integration VLSI 99 which was sponsored by the International Federation for Information Processing IFIP and was held in Lisbon Portugal in December 1999 The volume is organized around two themes in which the following topics are addressed VLSI Systems Design and Applications Analog Systems Design Analog Modeling and Design Image Processing Reconfigurable Computing Memory and System Design Low Power Design VLSI Design Methods and CAD Test and Verification Analog CAD and Interconnect Fundamental CAD Algorithms Verification and Simulation CAD for Physical Design High Level Synthesis and Verification of Embedded Systems VLSI Systems on a Chip is essential reading for researchers working on system integration design and CAD **Circular** ,1995 Interconnect-centric Circuit Modeling and Simulation for Giga-hertz VLSI Signal/power Integrity Applications Zonghao Chen,2004 **Proceedings of ASP-DAC/VLSI Design 2002** ,2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c **High-Performance Digital VLSI Circuit Design** Richard X. Gu,Khaled M. Sharaf,Mohamed I. Elmasry,1996 High Performance Digital VLSI Circuit Design is devoted to the analysis and design of digital VLSI CMOS bipolar and BiCMOS circuits which are optimized for high performance applications The book starts by reviewing important background information in the area of MOS and bipolar device design and modeling Detailed analysis and design of high performance CMOS CML ECL NTL and BiCMOS circuits is given Achieving high speed while maintaining low power dissipation in digital circuits is addressed in depth in separate chapters The book ends with a sample application area of high performance design namely the design of phase locked loops The book can be used as a reference for practicing IC designers and as a text for graduate and senior undergraduate students in the area of digital IC design **JJAP** ,2010 Digital Timing Macromodeling for VLSI Design Verification Jeong-Taek

Kong, David V. Overhauser, 1995-05-31 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques

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