

POWER OPTIMIZATION AND SYNTHESIS AT BEHAVIORAL AND SYSTEM LEVELS USING FORMAL METHODS



Jui-Ming Chang
Massoud Pedram

Kluwer Academic Publishers

Power Optimization And Synthesis At Behavioral And System Levels Using Formal Methods

Wai-Kai Chen

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Chang, Massoud Pedram, 2012-12-06 Integrated circuit densities and operating speeds continue to rise at an exponential rate. Chips however cannot get larger and faster without a sharp decrease in power consumption beyond the current levels. Minimization of power consumption in VLSI chips has thus become an important design objective. In fact with the explosive growth in demand for portable electronics and the usual push toward more complex functionality and higher performance, power consumption has in many cases become the limiting factor in satisfying the market demand. A new generation of power conscious CAD tools are coming onto the market to help designers estimate, optimize and verify power consumption levels at most stages of the IC design process. These tools are especially prevalent at the register transfer level and below. There is a great need for similar tools and capabilities at the behavioral and system levels of the design process. Many researchers and CAD tool developers are working on high level power modeling and estimation as well as power constrained high level synthesis and optimization. Techniques and tools alone are however insufficient to optimize VLSI circuit power dissipation; a consistent and convergent design methodology is also required. *Power Optimization and Synthesis at Behavioral and System Levels Using Formal Methods* was written to address some of the key problems in power analysis and optimization early in the design process. In particular, this book focuses on power macro modeling based on regression analysis and power minimization through behavioral transformations, scheduling, resource assignment and hardware/software partitioning and mapping. What differentiates this book from other published work on the subject is the mathematical basis and formalism behind the algorithms and the optimality of these algorithms subject to the stated assumptions. From the Foreword: This book makes an important contribution to the field of system design technologies by presenting a set of algorithms with guaranteed optimality properties that can be readily applied to system level design. This contribution is timely because it fills the need of new methods for a new design tool generation which supports the design of electronic systems with even more demanding requirements. Giovanni De Micheli, Professor, Stanford University.

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system levels of the design process Many researchers and CAD tool developers are working on high level power modeling and estimation as well as power constrained high level synthesis and optimization Techniques and tools alone are however insufficient to optimize VLSI circuit power dissipation a consistent and convergent design methodology is also required Power Optimization and Synthesis at Behavioral and System Levels Using Formal Methods was written to address some of the key problems in power analysis and optimization early in the design process In particular this book focuses on power macro modeling based on regression analysis and power minimization through behavioral transformations scheduling resource assignment and hardware software partitioning and mapping What differentiates this book from other published work on the subject is the mathematical basis and formalism behind the algorithms and the optimality of these algorithms subject to the stated assumptions From the Foreword This book makes an important contribution to the field of system design technologies by presenting a set of algorithms with guaranteed optimality properties that can be readily applied to system level design This contribution is timely because it fills the need of new methods for a new design tool generation which supports the design of electronic systems with even more demanding requirements Giovanni De Micheli Professor Stanford University

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits Saraju P. Mohanty, Nagarajan Ranganathan, Elias Kougianos, Priyadarsan Patra, 2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits

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