

Hardware Software Codesign of DSP System Using Grammar Based Approach

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Abstract

Embedded cores are gaining widespread use to deal with the complex DSP systems where flexibility is of utmost importance. The design of such a system offers several problems, which is not addressed by the existing methodology. The authors previously presented an integrated grammar based DSP design methodology that separates architectural and functional specification, can create a virtual prototype and has a smooth link to the implementation phase. In this paper we present the extension of the work to handle embedded cores. Here we capture the Host Peripheral Interface (HPI) of TMS320C6x core at higher level of abstraction and provide a single simulation environment, which facilitates faster analysis of hardware software components. Our results reveal that the proposed methodology offers simulation time speed-up of 5 times and design time speed-up of 8 times, while keeping the architectural specification separated from functionality.

1. Introduction

To cope with the complexity and gain flexibility to adapt to changing requirements, specialized systems often use a specific hardware platform in conjunction with a software part. This is further aided by the fact that shrinking geometry and accompanying increase in performance in many instances allow functions to be implemented in software that earlier required implementation in hardware. Hence, embedded cores are great system design components to gain flexibility but they pose design problems that are not well addressed by existing methodology.

The current practice of embedded system design starts with a written specification of the product

that is passed to the architectural design team. The team then carries out a manual partitioning into chips or chipsets, writes a primary specification for the device and hand it over to chip development team. The team then starts with RTL coding to implement the chip while the algorithmic modeling is done in C or C++ [1]. But RTL level is too detailed to be efficient enough to meet the time to market requirement. Thus HW/SW repartitioning, substituting better programmable VCs or custom hardware accelerator for part of the software become rather difficult. Therefore, if a design needs to evolve to deal with the next generation of products, we need to capture an embedded system at the highest level of abstraction.

The authors have presented a grammar based DSP design methodology called MASIC, Maths to ASIC [2,3]. Here we present the extension of our work to make MASIC capable of handling embedded cores while keeping the architectural specification apart from the DSP functionality. The benefits of such an approach are:

- Separation of architectural specification from DSP functionality makes it convenient to amend the design with different product family.
- This methodology captures the architecture using grammar notation and dataflow using C function that facilitates the designer to explore the design with different HW/SW combination.
- It allows concurrent development of architecture and dataflow that is highly desirable in industry to meet time to market requirements.
- Our results show that it offers simulation time speed-ups along with reduction in design time.

This paper illustrates the methodology and quantifies the results. In the next section we present related works in embedded system design.

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Donald E. Thomas, Rolf Ernst



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