

POWER AWARE DESIGN METHODOLOGIES

**Edited by
Massoud Pedram
Jan Rabaey**

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Power Aware Design Methodologies

Ravishankar Rao



Power Aware Design Methodologies:

Power Aware Design Methodologies Massoud Pedram, Jan M. Rabaey, 2014-01-15 Power Aware Design Methodologies Massoud Pedram, Jan M. Rabaey, 2007-05-08 Power Aware Design Methodologies was conceived as an effort to bring all aspects of power aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology circuit logic and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits, digital and analog systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in-depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends, this book provides a myriad of state-of-the-art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The contributors have reported the various technologies, methodologies, and techniques in such a way that they are understandable and useful.

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis Sumit Ahuja, Avinash Lakshminarayana, Sandeep Kumar Shukla, 2011-10-22 This book presents novel research techniques, algorithms, methodologies, and experimental results for high-level power estimation and power-aware high-level synthesis. Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low-power ASIC/FPGA design.

Low Power Networks-on-Chip Cristina Silvano, Marcello Lajolo, Gianluca Palermo, 2010-09-24 In recent years, both Networks-on-Chip as an architectural solution for high-speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities. This book offers a single source reference to some of the most important design techniques proposed in the context of low-power design for networks-on-chip architectures.

Micropower Digital Design Techniques for the Nanometer Realm Robert Matthew Senger, 2008

Low-Power Design and Power-Aware Verification Progyna Khondkar, 2017-10-05 Until now, there has been a lack of a complete knowledge base to fully comprehend Low-power LP design and power-aware PA verification techniques and methodologies and deploy them all together in a real design verification and implementation project. This book is a first approach to establishing a comprehensive PA knowledge base. LP design, PA verification, and Unified Power Format (UPF) or IEEE 1801 power format standards are no longer special features. These technologies and methodologies are now part of industry standard design verification and implementation flows. DVIF: Almost every chip design today incorporates some kind of low-power technique, either through power management on-chip by dividing the design into different voltage areas and controlling the voltages through PA dynamic and PA static verification or their combination. The entire LP design and PA verification process involves thousands of techniques, tools, and methodologies employed from the register transfer level (RTL) of design abstraction down to the synthesis or place-and-route levels of physical design. These

techniques tools and methodologies are evolving everyday through the progression of design verification complexity and more intelligent ways of handling that complexity by engineers researchers and corporate engineering policy makers

Power-Aware Testing and Test Strategies for Low Power Devices Patrick Girard,Nicola Nicolici,Xiaoqing Wen,2010-03-11 Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry Elaborate power management strategies such as dynamic voltage scaling clock gating or power gating techniques are used today to control the power dissipation during functional operation The usage of these strategies has various implications on manufacturing test and power aware test is therefore increasingly becoming a major consideration during design for test and test preparation for low power devices This book explores existing solutions for power aware test and design for test of conventional circuits and systems and surveys test strategies and EDA solutions for testing low power devices **Integrated Circuit and System Design** ,2005 On-chip Communication Kanishka Lahiri,2003 Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology ,2007 **HLSpower** Ravishankar Rao,2002 **Algorithms and Data Structures** ,2005 **International Symposium on Quality Electronic Design** ,2002 Annotation Fifty one papers and 21 posters from the March 2002 symposium report current research in deep submicron integrated circuit design and development The sessions address interconnect extraction and modeling design for process variations metrics power and noise management verification signal integrity and low power design techniques Some of the topics are transition aware global signaling TAGS the interoperability of EDA tools for sequential logic synthesis statistical methods for the determination of process corners power supply noise suppression via clock skew scheduling and the relation between SAT and BDDs for equivalence checking No subject index Annotation copyrighted by Book News Inc Portland OR **Annual IEEE Semiconductor Thermal Measurement and Management Symposium** ,2005 **Proceedings of the ... International Symposium on Hardware/Software Codesign** ,2001 *ISLPED'03* ,2003 *Modeling and Microarchitecture for Low Power* Ravishankar V. Rao,2006 *Fourth International Symposium on Quality Electronic Design* ,2003 ISQED looks into the research development and application of design techniques and methods design processes and EDA design methodologies and tools that address issues that impact the quality of the realization of designs into physical integrated circuits It emphasizes a holistic approach toward design quality and to highlight and accelerate cooperation among the IC Design EDA Semiconductor Process Technology and Manufacturing communities Proceedings ,2005 **Energy Efficient Data Management Techniques in Wireless Sensor Networks** Haiyang Liu,2007

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