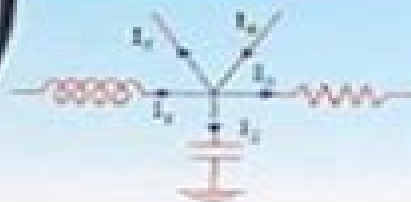


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**Principles of Circuit and  
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# Principles Of Circuit And Interconnect Simulation

**Arturo Cuomo**



## **Principles Of Circuit And Interconnect Simulation:**

**Modeling and Simulation of High Speed VLSI Interconnects** Michel S. Nakhla, Q.J. Zhang, 2011-06-28 Modeling and Simulation of High Speed VLSI Interconnects brings together in one place important contributions and state of the art research results in this rapidly advancing area Modeling and Simulation of High Speed VLSI Interconnects serves as an excellent reference providing insight into some of the most important issues in the field *Circuit Simulation Principles and Techniques and Their Application Toward Interconnect Simulation* Kirk Alan Ingemunson, 1994

**On-Chip Inductance in High Speed Integrated Circuits** Yehea I. Ismail, Eby G. Friedman, 2012-12-06 The appropriate interconnect model has changed several times over the past two decades due to the application of aggressive technology scaling New more accurate interconnect models are required to manage the changing physical characteristics of integrated circuits Currently RC models are used to analyze high resistance nets while capacitive models are used for less resistive interconnect However on chip inductance is becoming more important with integrated circuits operating at higher frequencies since the inductive impedance is proportional to the frequency The operating frequencies of integrated circuits have increased dramatically over the past decade and are expected to maintain the same rate of increase over the next decade approaching 10 GHz by the year 2012 Also wide wires are frequently encountered in important global nets such as clock distribution networks and in upper metal layers and performance requirements are pushing the introduction of new materials for low resistance interconnect such as copper interconnect already used in many commercial CMOS technologies On Chip Inductance in High Speed Integrated Circuits deals with the design and analysis of integrated circuits with a specific focus on on chip inductance effects It has been described throughout this book that inductance can have a tangible effect on current high speed integrated circuits For example neglecting inductance and using an RC interconnect model in a production 0.25  $\mu\text{m}$  CMOS technology can cause large errors over 35% in estimates of the propagation delay of on chip interconnect It has also been shown that including inductance in the repeater insertion design process as compared to using an RC model improves the overall repeater solution in terms of area power and delay with average savings of 40.8%, 15.6% and 6.7% respectively On Chip Inductance in High Speed Integrated Circuits is full of design and analysis techniques for RLC interconnect These techniques are compared to techniques traditionally used for RC interconnect design to emphasize the effect of inductance

**On-Chip Inductance in High Speed Integrated Circuits** will be of interest to researchers in the area of high frequency interconnect noise and high performance integrated circuit design

**Circuit Analysis, Simulation and Design** Albert E. Ruehli, 1987 This book covers algorithmic aspects of computer aided circuit design for VLSI of large circuits The large scale aspect of VLSI requires a reorientation towards new and more efficient techniques Many algorithms have survived the test of time while others are suffering from the usual problem of polynomial or exponential running time complexity and storage requirements The approaches presented in this book are techniques which were developed in response to the VLSI problems

The most recent exact circuit analysis and simulation techniques are presented such as waveform relaxation and timing simulation. The book concentrates on the analysis and simulation of large circuits which exceed the capabilities of general purpose analyzers in both compute time and storage. Also discussed are circuit models for switch level simulation techniques and circuit models for interconnections capacitance and inductances and optimization techniques. The language and notation have been kept uniform throughout the book to help the reader to maintain the continuity between the topics discussed in the different chapters. All algorithms are written in a Pascal style. The terminology used should reflect the emerging language used in most of the VLSI circuit design community. The book includes proven approaches as well as techniques which are presently in a research state.

*Modeling and Testing of Electromigration Effects in Integrated Circuit Interconnects and Contacts Under Time-varying Current Conditions* Boon-Khim Liew, 1990      **Official Gazette of the United States Patent and Trademark Office** United States. Patent and Trademark Office, 2001      **Electronic Materials Handbook**, 1989-11-01

Volume 1 Packaging is an authoritative reference source of practical information for the design or process engineer who must make informed day to day decisions about the materials and processes of microelectronic packaging. Its 117 articles offer the collective knowledge, wisdom and judgement of 407 microelectronics packaging experts, authors, co-authors and reviewers representing 192 companies, universities, laboratories and other organizations. This is the inaugural volume of ASMAs all new Electronic Materials Handbook series designed to be the Metals Handbook of electronics technology. In over 65 years of publishing the Metals Handbook, ASM has developed a unique editorial method of compiling large technical reference books. ASMAs access to leading materials technology experts enables to organize these books on an industry consensus basis. Behind every article is an author who is a top expert in its specific subject area. This multi-author approach ensures the best, most timely information throughout. Individually selected panels of 5 and 6 peers review each article for technical accuracy, generic point of view and completeness. Volumes in the Electronic Materials Handbook series are multidisciplinary to reflect industry practice applied in integrating multiple technology disciplines necessary to any program in advanced electronics. Volume 1 Packaging, focusing on the middle level of the electronics technology size spectrum, offers the greatest practical value to the largest and broadest group of users. Future volumes in the series will address topics on larger integrated electronic assemblies and smaller semiconductor materials and devices size levels.

*Behavioral Modeling and Simulation of Analog Circuits* Junjie Yang, 2005      *Proceedings*, 2004      *Science Abstracts*, 1993      **Annual Connectors and Interconnection Technology Symposium Proceedings**, 1989      *International Conference on Simulation of Semiconductor Processes and Devices*, 1999      *IEEE Circuits & Devices*, 1995      **Simulation Digest**, 1994      **Proceedings of the ... ACM Great Lakes Symposium on VLSI**, 2007      *19th IEEE VLSI Test Symposium*, 2001. Collects 58 papers from the April-May 2001 symposium that explore new approaches in the testing of electronic circuits and systems. Key areas in testing are discussed such as BIST, analog measurement, fault tolerance, diagnosis.

methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc

**Nanoelectronic Mixed-Signal System Design** Saraju Mohanty, 2015-02-20 Covering both the classical and emerging nanoelectronic technologies being used in mixed signal design this book addresses digital analog and memory components Winner of the Association of American Publishers 2016 PROSE Award in the Textbook Physical Sciences Mathematics category Nanoelectronic Mixed Signal System Design offers professionals and students a unified perspective on the science engineering and technology behind nanoelectronics system design Written by the director of the NanoSystem Design Laboratory at the University of North Texas this comprehensive guide provides a large scale picture of the design and manufacturing aspects of nanoelectronic based systems It features dual coverage of mixed signal circuit and system design rather than just digital or analog only Key topics such as process variations power dissipation and security aspects of electronic system design are discussed Top down analysis of all stages from design to manufacturing Coverage of current and developing nanoelectronic technologies not just nano CMOS Describes the basics of nanoelectronic technology and the structure of popular electronic systems Reveals the techniques required for design excellence and manufacturability

**EUROCON** ,1986      Ceramic Interconnect Technology ,2003

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